A Remark on Nearly Planar Embeddings of Small Ultracomputers

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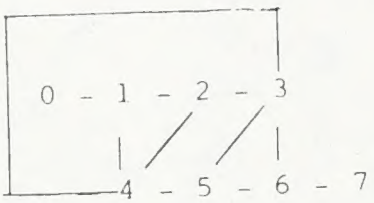
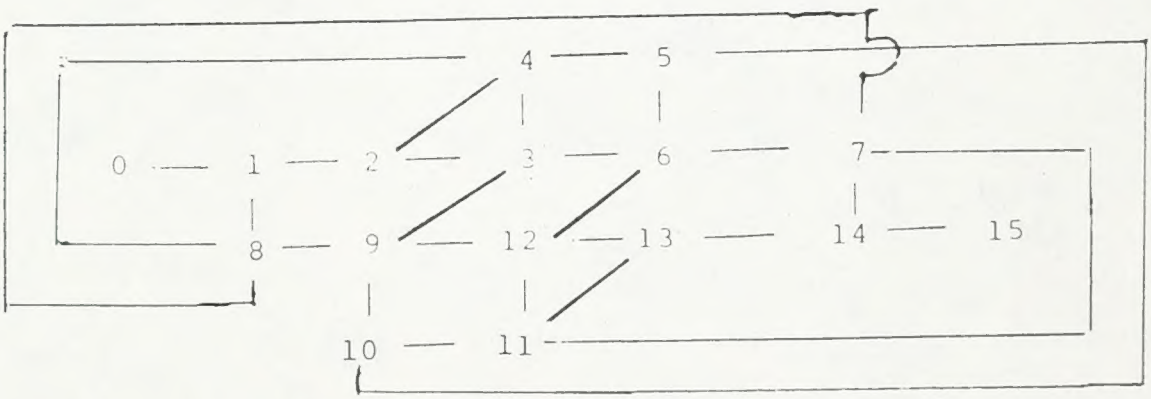
Ultracomputer Note #4

December 2, 1979

For efficient VLSI realizations of ultracomputers, planar or nearly planar realizations of the shuffle interconnection are desirable. In the N=8 case this is easily done as follows:



In the N=16 case the following nearly planar layout is available:



This graph is not planar, since it contains the Kuratowski ('three houses and three wells') graph as a subgraph, namely:

6 connects to (3, 12, 7)
9 connects to (3, 12, 7 via 8)
11 connects to (3via10via5via4, 12, 7).

It would be interesting to study the genesis of the perfect shuffle connection graphs for higher values of N.